Notice of Allowability	Application No.	Applicant(s)	
	09/876,848	HUANG ET AL.	
	Examiner	Art Unit	
	Jacqueline Wilson	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment received 10/28/04*.

2. ☒ The allowed claim(s) is/are *1-7,9-25,27 and 28*.

3. ☒ The drawings filed on *09 April 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-7, 9-25 and 27-28 are allowed.

The prior art neither teaches nor fairly suggests a method comprising selecting a row from a plurality of rows in a pixel array, opening a path between a first line having a first voltage and a bus through one or more row select transistors, selecting the row for reset, opening a path between a second line having a second voltage and the bus through one or more reset enable transistors, the second voltage being higher than the first voltage, and **providing the second voltage to the one or more row select transistors**, as claimed in Claim 1. New claim 28 is substantially similar to Claim 1.

The prior art neither teaches nor fairly suggests a bus, a first line operative to carry a select voltage, a second line operative to be driven to a boosted voltage, the boosted voltage being higher than the select voltage, and **a first circuit operative to couple the bus to the first line in response to a row select signal**, the first circuit including **a transistor coupled to the second line**, wherein **the boosted voltage comprises a reset enable signal**, as claimed in Claim 5.

The prior art neither teaches nor fairly suggests a bus, a first line operative to carry a select voltage, a second line operative to be driven to a boosted voltage, the boosted voltage being higher than the select voltage, a first circuit

operative to be driven to a boosted voltage, the boosted voltage being higher than the select voltage, **a first circuit operative to couple the bus to the first line in response to a row select signal, the first circuit including a transistor coupled to the second line**, and **a second circuit operative to couple the bus to the second line in response to a row reset signal**, as claimed in Claim 6.

The prior art neither teaches nor fairly suggests a bus, a first line operative to carry a select voltage, a second line operative to be driven to a boosted voltage, the boosted voltage being higher than the select voltage, and **a first circuit operative to couple the bus to the first line in response to a row select signal**, the first circuit including **a transistor coupled to the second line**, wherein **the transistor is coupled to the second line such that there is no parasitic diode leakage between the first line and the second line through the transistor in response to the second line being driven to the boosted voltage**, as claimed in Claim 7.

The prior art neither teaches nor fairly suggests a bus, a first line operative to carry a select voltage, a second line operative to be driven to a boosted voltage, the boosted voltage being higher than the select voltage, and **a first circuit operative to couple the bus to the first line in response to a row select signal**, the first circuit including **a transistor coupled to the second line**, wherein **the bus comprises a shared row-reset bus**, as claimed in Claim 15.

The prior art neither teaches nor fairly suggests a pixel array including a plurality of pixels arranged in rows and columns, a plurality of buses, each bus coupled to pixels in one row of the pixel array, a first line operative to carry a select voltage, a second line operative to carry a row enable voltage, a charge pump boost circuit operative to drive the second line to a boosted voltage, the boosted voltage being higher than the select voltage, a plurality of row drivers, each row driver coupled to an associated one of the buses and **including a first circuit operative to couple the bus to the first line in response to a row select signal, the first circuit including a transistor coupled to the second line**, wherein **the bus comprises a shared row-reset bus**, as claimed in Claim 16.

The prior art neither teaches nor fairly suggests a pixel array including a plurality of pixels arranged in rows and columns, a plurality of buses, each bus coupled to pixels in one row of the pixel array, a first line operative to carry a select voltage, a second line operative to carry a row enable voltage, a charge pump boost circuit operative to drive the second line to a boosted voltage, the boosted voltage being higher than the select voltage, a plurality of row drivers, each row driver coupled to an associated one of the buses and **including a first circuit operative to couple the bus to the first line in response to a row select signal, the first circuit including a transistor coupled to the second line, and a second circuit operative to couple the bus to the second line in response to a row reset signal**, as claimed in Claim 17.

The prior art neither teaches nor fairly suggests a pixel array including a plurality of pixels arranged in rows and columns, a plurality of buses, each bus coupled to pixels in one row of the pixel array, a first line operative to carry a select voltage, a second line operative to carry a row enable voltage, a charge pump boost circuit operative to drive the second line to a boosted voltage, the boosted voltage being higher than the select voltage, a plurality of row drivers, each row driver coupled to an associated one of the buses and **including a first circuit operative to couple the bus to the first line in response to a row select signal, the first circuit including a transistor coupled to the second line, wherein the transistor is coupled to the second line such that there is no parasitic diode leakage between the first line and the second line through the transistor in response to the second line being driven to the boosted voltage,** as claimed in Claim 18.

The prior art neither teaches nor fairly suggests a pixel array including a plurality of pixels arranged in rows and columns, a plurality of buses, each bus coupled to pixels in one row of the pixel array, a first line operative to carry a select voltage, a second line operative to carry a row enable voltage, a charge pump boost circuit operative to drive the second line to a boosted voltage, the boosted voltage being higher than the select voltage, a plurality of row drivers, each row driver coupled to an associated one of the buses and **including a first circuit operative to couple the bus to the first line in response to a row select signal, the first circuit including a transistor coupled to the second**

line, wherein the boosted voltage comprises a reset enable signal, as claimed in Claim 19.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacqueline Wilson whose telephone number is (571) 272-7322. The examiner can normally be reached on 8:30am-5:00pm (alternate Fridays off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on (571) 272-7308. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JW
04/06/05

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